

Appl. No. 10/707,398
Amdt. dated December 03, 2004
Reply to Office action of November 17, 2004

Amendments to the Specification:

Please substitute Paragraph [0005] with the following amended test:

5 Please refer to Fig.1 and Fig.2. Fig.1 is an enlarged top view of a part of a conventional test key layout for monitoring GC-DT (Gate Conductor-Deep Trench) misalignment during the fabrication of deep trench capacitors of a trench capacitor DRAM device. Fig.2 is a schematic cross-sectional diagram showing the test key structure along line N-N of Fig.1. As shown in Fig.1, the test key layout 1 is fabricated on
10 a silicon substrate 10, usually within a scribe line area. The test key layout 1 comprises two adjacent deep trench capacitors 11 and 12 electrically connecting to each other through out diffusions 30 therebetween. The deep trench capacitors 11 and 12 of the test key layout 1 are fabricated simultaneously with those deep trench capacitors arranged in the memory array using the same fabrication processes. Therefore, the structure of each
15 of the deep trench capacitors 11 and 12 and the structure of each of the deep trench capacitors in the memory array are substantially the same. Basically, as best seen in Fig.2, each of the deep trench capacitors 11 and 12, which are embedded into a main surface of the silicon substrate 10, comprises a buried plate 111, a capacitor dielectric 112, storage node 113, and oxide collar 114. The storage node 113 of the deep trench capacitor 11 and
20 the storage node 113 of the deep trench capacitor 12 are electrically connected to each other through the overlapping out diffusions 30. A cap insulation layer 115 is disposed atop each of the deep trench capacitors 11 and 12. A plurality of gate conductor (GC) lines overlays the deep trench capacitors 11 and 12. As specifically indicated in Fig.1, these GC lines are alternately denoted by "T" and "B", wherein "T" stands for a top GC line (GC-T) and "B" stands for a bottom GC line (GC-B). The plurality of GC lines
25 including GC-T and GC-B are arranged in column on the main surface of the silicon

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substrate 10. The ~~GC-T 201~~-GC-B 201 is disposed at one side of the deep trench capacitor 11. The ~~GC-B 202~~-GC-T 202 runs over the deep trench capacitor 11. The ~~GC-T 203~~-GC-B 203 runs over the deep trench capacitor 12. The ~~GC-B 204~~-GC-T 204 is
5 disposed at one side of the deep trench capacitor 12.

Please substitute Paragraph [0006] with the following amended test:

As best seen in Fig.2, the ~~GC-T 201~~-GC-B 201 acts as a switching transistor of the deep trench capacitor 11. The ~~GC-B 204~~-GC-T 204 acts as a switching transistor of the deep trench capacitor 12. Heavily doped source/drain 301 is implanted into the silicon
10 substrate 10 at both sides of each of the ~~GC-T 201~~-GC-B 201 and ~~GC-B 204~~-GC-T 204. According to the prior art method, to assess the GC-DT misalignment, the threshold voltage (V_{TH}) shifts of the ~~GC-T 201~~-GC-B 201 and ~~GC-B 204~~-GC-T 204 are measured as known to those skilled in the art. However, the prior art GC-DT misalignment evaluation method is not accurate because there are so many factors affecting the
15 threshold voltages shift of the ~~GC-T 201~~-GC-B 201 and ~~GC-B 204~~-GC-T 204. Some of these factors include narrow GC line width, thermal budget of ion implantation, and GC sidewall etching. Therefore, it is difficult for an inspector to judge the GC-DT misalignment merely according to the measured threshold voltage shift data. Consequently, there is a need to provide an improved wafer acceptance testing method for
20 accurately monitoring GC-DT misalignment.

Please substitute Paragraph [0027] with the following amended test:

Referring to Fig.9, the GC-DT misalignment case is demonstrated. It is mentioned that in an ideal aligned case as set forth in Fig.8 the capacitance between the GC finger 740 and the out diffusion 630 and the capacitance between the GC finger 860 and the out
25 diffusion 630 may be omitted because of thick STI 601 and trench top oxide. In Fig.9,

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since the GC-DT misalignment occurs, the GC finger 860, which is supposed to be laid on the STI, now shifts to the right and thus partially overlapping with the out diffusion 603 adjacent to the elongated finger deep trench portion 26 (indicated by the circle region). All of the GC fingers in the test key layout have the same shift. Therefore, the GC finger 840 is now closer to the N^+ out diffusion 630 adjacent to the elongated finger deep trench portion 24 (indicated by the circle region), while the GC finger 760 is more space apart from the N^+ out diffusion 630 adjacent to the elongated finger deep trench portion 26. This results in a larger capacitance of C1 and smaller capacitance of C2 ($C1 > C2$). From above, it is easy to assess the GC-DT misalignment by comparing the capacitances of C1 and C2. If capacitance C1 . capacitance C2, GC-DT ~~misaligns~~ is misaligned.

Please substitute Abstract with the following amended text:

A wafer acceptance testing (WAT) method for monitoring GC-DT misalignment and a test key structure are disclosed. The test key includes a deep trench capacitor structure biased to a first voltage (V_{DT}). ~~The deep trench capacitor structure is formed in a substrate, on which active areas are defined. The deep trench capacitor structure includes a buried strap out diffusion region that is formed within the active area and is electrically connected to the deep trench capacitor structure. The deep trench capacitor structure is isolated by shallow trench isolation (STI). A GC-T electrode layout and a GC-B electrode layout are formed over the substrate. The A GC-T electrode layout, which is biased to a second voltage (V_{GC-T}), includes a plurality of columns of GC-T fingers. The A GC-B electrode layout, which is biased to a third voltage (V_{GC-B}), includes a plurality of columns of GC-B fingers that interdigitate the plurality of columns of GC-T fingers over the active areas and STI. A first capacitance C_1 of a first capacitor contributed by the plurality of columns of GC-T fingers and the buried strap out diffusion region is~~

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measured. A second capacitance C_2 of a second capacitor contributed by the plurality of columns of GC-B fingers and the buried strap out diffusion region is measured. The first capacitance C_1 and second capacitance C_2 are compared, wherein when $C_1 \neq C_2$, GC-DT
5 is misaligned.